Remarks

The Official Action rejected claims 1-4, 10-12, 27 and 39-48. Applicant has amended claims 1, 27, 43, 46 and 48, and canceled claims 11, 41, 45 and 47. Reconsideration and allowance of the pending claims are respectfully requested.

Claim Rejections under 35 USC 102

The Official Action rejected claims 27, 40 and 41 under 35 USC 102(e) as being anticipated by Walker et al. (US Patent 6,845,472). Applicant respectfully requests reconsideration and withdrawal of the present rejection.

As is well-established, in order to successfully assert a prima facie case of anticipation, the Office Action must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Therefore, if even one element or limitation is missing from the cited document, the Office Action has not succeeded in making a prima facie case.

Each of claims 27, 40 and 41 recites a first memory device having a first storage array ....., a first memory error logic to carry out a check for memory errors within the first storage array under at least one condition comprising ..... during an idle period associated with transactions carried out by the memory controller on the first memory bus that involve the first storage array, and a first bus error logic associated with the first interface buffer to carry out a check for bus errors in transactions on the first memory bus between the memory controller and the first interface, is unanticipated by Walker.

It is unclear from the Office Action that which device of Walker is regarded as the first memory device and which device of Walker is regarded as the memory

controller of claims 27, 40 and 41, which adds difficulties for Applicant to argue for the novelty of claims 27, 40, 41.

In order to expedite the examination, Applicant provides the following arguments under various assumptions for the memory controller and the first memory device of claims 27, 40 and 41:

1) If DIMMs 44 are regarded as the first memory device and memory control devices 48a-e are regarded as the memory controller, Claims 27, 40 and 41 are unanticipated by Walker because Walker teaches the memory controller devices 48a-e, the error detection and correction devices 62a-e and the RAID memory engine 64 can be used to detect and correct the data read from DIMMs 44 (see column 8, lines 54-63), but not a memory error logic of DIMMs 44 to correct the data. In other words, Walker does not teach DIMMs 44 have a memory error logic to check for memory errors within the storage arrays of themselves. Therefore, Walker does not anticipate claims 27, 40 and 41.

2) If memory sub-system 40 is regarded as the first memory device and host controller 58 is regarded as the memory controller, claims 27, 40 and 41 are unanticipated by Walker because Walker teaches the memory errors are checked in response to a READ command from host controller 58. Although cleansing logic 70 of memory sub-system 40 initiates an internal READ command to check specified regions of the memory sub-system 40 during periods when there are no READ/WRITE requests from external devices, there is still a transaction between host controller 58 and memory sub-system 40 since the internal READ command is sent from cleansing logic 70 to memory cartridge 42a-e through arbitrator 72 of host controller 58 (see column 8, lines 34-48). In other words, Walker does not teach checking memory errors during an idle period associated with transactions between

the memory controller and the memory device. Therefore, Walker does not anticipate claims 27, 40 and 41.

Moreover, although Walker teaches a scheme for memory error detection and correction, it is silent on checking bus errors in transactions on the memory bus between the memory controller and the memory device. It appears that the Office Action (see rejection of claim 41) relies on column 7, lines 45-57 of Walker for the teaching of bus error checking. Applicant respectfully submits that the cited part of Walker talks about checking single-bit errors of the data retrieved from memory cartridge 42a-e by detection and correction devices 62a-e. It can be seen that the single-bit errors are related to the data from the memory device, which should reflect the memory errors, but not the bus errors as requested by claims 27, 40 and 41. Definition of single errors is given in column 1, lines 35-67 of Walker. Especially, lines 63-67 of column 1 define that "memory errors can be categorized as either single-bit or multi-bit errors. A single bit error refers to an error in a single memory cell."

Since Walker does not teach each and every limitation of claims 27, 40 and 41, Walker does not anticipate the invention of claims 27, 40 and 41. Applicant respectfully requests the rejection of claims 27, 40 and 41 be withdrawn.

Claim Rejections under 35 USC 103 (Vogt/Walker/Goris)

The Official Action rejected claims 1-4, 10-12, 39 and 46-48 under 35 USC 103(a) as being unpatentable over Vogt (US Patent Application 2004/0260991) in further view of Dell (US Patent 6,349,390) and Walker.

As is well established, a prima facie showing of obviousness may only be established if there is a clear suggestion from or in the prior art to make the

modifications proposed by the Examiner. See Gillette Co. v. S.C. Johnson & Son, Inc. 919 F. 2d 720 (Fed Cir. 1990). As discussed in MPEP 2143.01, the prior art must suggest the desirability of the claimed invention.

The Office Action deems that Vogt teaches every elements and limitations of claim 1 except that the error checking is carried out in response to a read command and during an idle period associated with transactions carried out by the memory controller that involve the storage array, which are disclosed by Dell and Walker. The desirability of the combination as deemed is also suggested by Dell and Walker, namely, to decrease the number of errors without lowering system efficiency.

Applicant respectfully submits that Vogt is related to a memory channel utilizing permuting status patterns. Vogt is silent on checking and correcting memory errors. Therefore, starting from Vogt, a skilled person does not have a motivation to combine Vogt with Dell and Walker in order to decrease the number of errors (i.e., memory errors) without lowering system efficiency.

It appears that the Office Action relies on paragraph 83 of Vogt for the teaching of carrying out a check for memory errors within the storage array. Applicant respectfully submits that paragraph 83 teaches a method of distinguishing a status frame from a data frame by utilizing a wrong CRC code, but not a method of checking memory errors. More particularly, paragraph 83 teaches a sending memory agent attaches a wrong CRC code to a status frame before sending it to a receiving memory agent, so that the receiving agent may interpret the frame as a status frame rather than a data frame once detecting that the CRC code attached to the frame is wrong. The sending memory agent may be a memory buffer of a sending memory module and the receiving memory agent may be a memory buffer of a receiving

memory module (see paragraph 84). It can be seen that paragraph 83 teaches nothing about memory error checking, saying nothing of memory error correction.

In lieu of above, starting from Vogt, a skilled person does not have a motivation to combine Vogt with Walker and Dell in order to decrease the number of errors (i.e., memory errors) without lowering system efficiency.

Moreover, as discussed in M.P.E.P 2143.03, to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Claim 1, which recites a memory device comprising bus error logic associated with the interface buffer to carry out a check for bus errors in transactions across the first memory bus between the memory controller and the first interface, is neither taught nor suggested by the combination of Vogt, Walker and Dell.

It appears that the Office Action (see rejection of claim 11) relies on column 3, lines 23-64 of Dell for the teaching of the bus error logic as requested by claim 1. Applicant respectfully submits that column 3, lines 23-64 of Dell teaches ECC unit 62 within bus control controller 34 which is design and can be structured as disclosed in US Pat No. 5,450, 422.

US Pat No. 5,450,422 discloses a SIMM memory including error correction for eight bytes of data, wherein the SIMM is configured to operate at a given speed for read and write operations. The SIMM comprises a logic to generate at least four check bits from the eight bits of each data byte written; ....; a logic to read each data byte and associated check bits from the DRAM and generate new check bits and

compare the newly-generated check bits with the stored check bits to correct and output all single-bit errors and detect some multi-bit errors in the read data and supply said corrected data to the system bus.

In lieu of above, US Pat No. 5,450,422 teaches a logic for checking and correcting memory errors in the data read from the SIMM memory, but not for checking bus errors in transactions across the memory bus between the memory controller and the memory device.

Therefore, Dell does not teach the bus error logic as requested by claim 1.

As conceded in the Office Action, Vogt fails to teach the bus error logic as requested by claim 1.

For similar reasons proffered for claims 27, 40 and 41, Walker does not teach the bus error logic as requested by claim 1.

Since a skilled person does not have a motivation to combine Vogt with Walker and Dell, and the combination does not teach each and every limitation of claim 1, claim 1 is patentable over Vogt in further view of Walker and Dell. Therefore, claim 1 is allowable and withdrawal of the present rejection is respectfully requested.

For similar reasons proffered for claim 1, claim 46 which recites a method, comprising: ....; checking whether bus errors occurred in a transmission of the read command across the memory bus by a bus error logic of the memory device;....; utilizing the check bit to check memory errors within the storage array, by a memory error logic of the memory device, is patentable over Vogt in further view of Walker and Dell. Therefore, claim 46 is allowable and withdrawal of the present rejection is respectfully requested.

Each of claims 2-4, 10-12, 39 and 47-48 includes one of claims 1 and 46 as a base claim. Accordingly, each of claims 2-4, 10-12, 39 and 47-48 is at least allowable for the reasons noted above.

Claim Rejections under 35 USC 103 (Walker/Goris)

The Official Action rejected claims 42-45 under 35 USC 103(a) as being unpatentable over Walker and Goris.

Claim 45 has been canceled. Claims 42-44 include claim 27 as a base claim. Therefore, claims 42-44 are allowable for the similar reason proffered for claim 27. Applicant respectfully requests reconsideration and withdrawal of the present rejection.

Conclusion

The foregoing is submitted as a full and complete response to the Official Action. Applicant submits that all remaining claims are in condition for allowance. Reconsideration is requested, and allowance of all remaining claims is earnestly solicited.

Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666. If the Examiner believes that there are any informalities which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (503) 439-8778 is respectfully solicited.

Respectively,

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